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 09/837007
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Class	Subclass
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ISSUE CLASSIFICATION

N

PATENT NUMBER

U.S. UTILITY Patent Application

O.I.P.E. SCANNED <u>14-3</u> G.A. <u>Am</u>	PATENT DATE
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APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/837007		257		<u>2827</u>	Mitchell

Applicants: Mou-Shiung Lin
 Ning-Ta Lin
 Chuen-Jye Lin

Title: Structure and manufacturing method of a chip scale package

PTO-2040
 12/99

[illegible]

<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS Sheets Dwg. Figs. Dwg. Print Fig.		CLAIMS ALLOWED	
			Total Claims	Print Claim for O.G.
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<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S. Patent No. _____ _____ _____			ISSUE FEE	
	_____ (Primary Examiner) _____ (Date)		Amount Due	Date Paid
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	_____ (Legal Instruments Examiner) _____ (Date)		ISSUE BATCH NUMBER	

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